Attackboard: A Novel Dependency-Aware Traffic Generator for Exploring NoC Design Space

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Motivation	Rebuild The State Machine	Overview of Attackboard	Evaluation Setup	
	Attackboard uses small tables to represent the state		Emulate ATG on Tilera TILE64	
Trace-driven simulation is simple and fast for exploring NoC design space.		Attackboard Traffic Generator (ATG)	Native processor Tilera TILE64 element	
For the consideration of accuracy, traces with packet dependencies is	machines	attackboard	Native processor 700 Mhz frequency	
necessarv.	How to do?	ATG 1 1 0 0 troffic	Simulated topology /x/ mesh network	

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However, these trace logs can be very complicated and require large storage space!

The BIG problem is size, while the conventional trace compression mechanism is not a good solution for reducing the size of traces while maintaining accuracy.

Key Question

How to reduce size of traces while maintaining accuracy?

Domain: NoC design space exploration

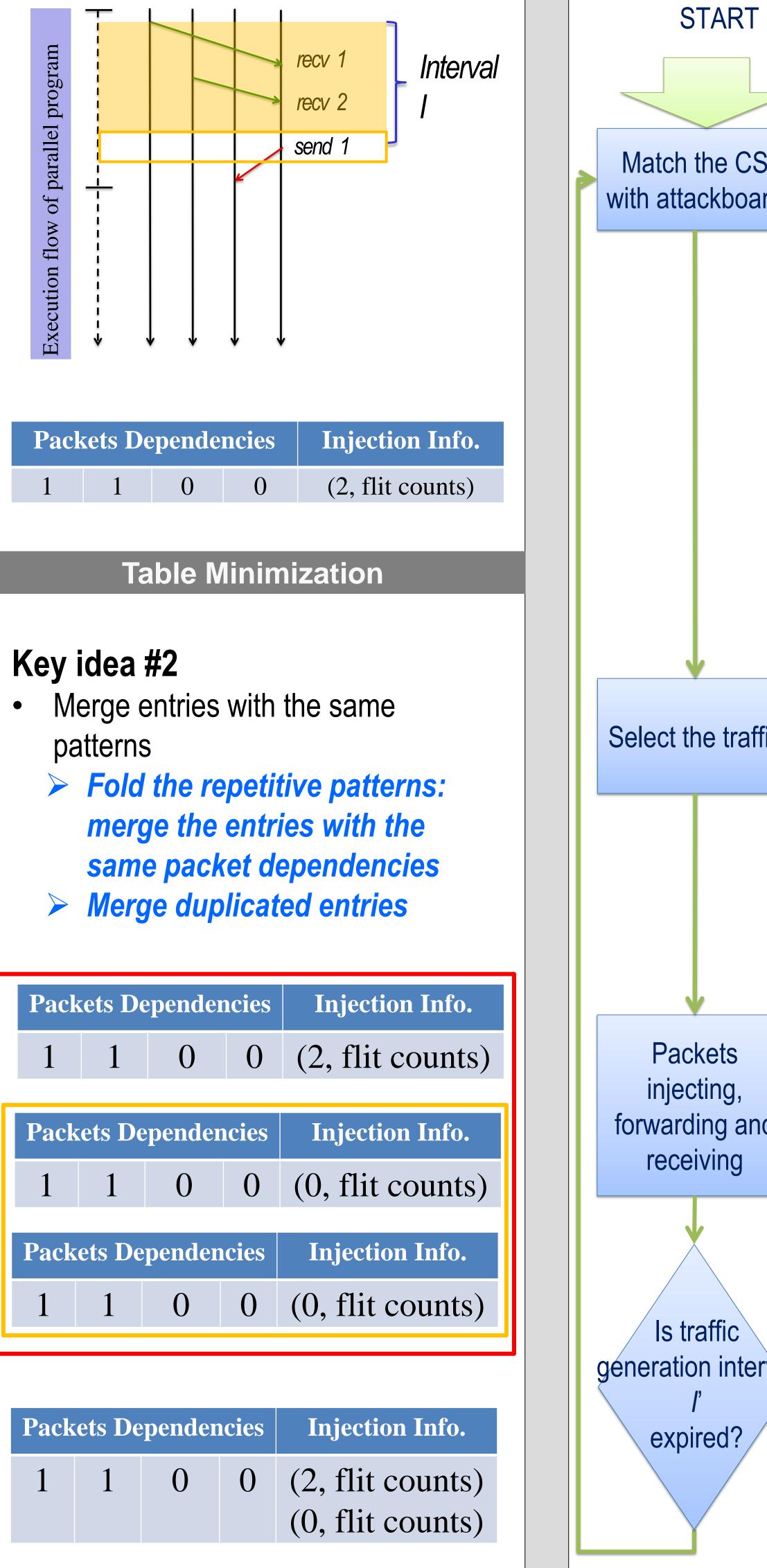
How to do?

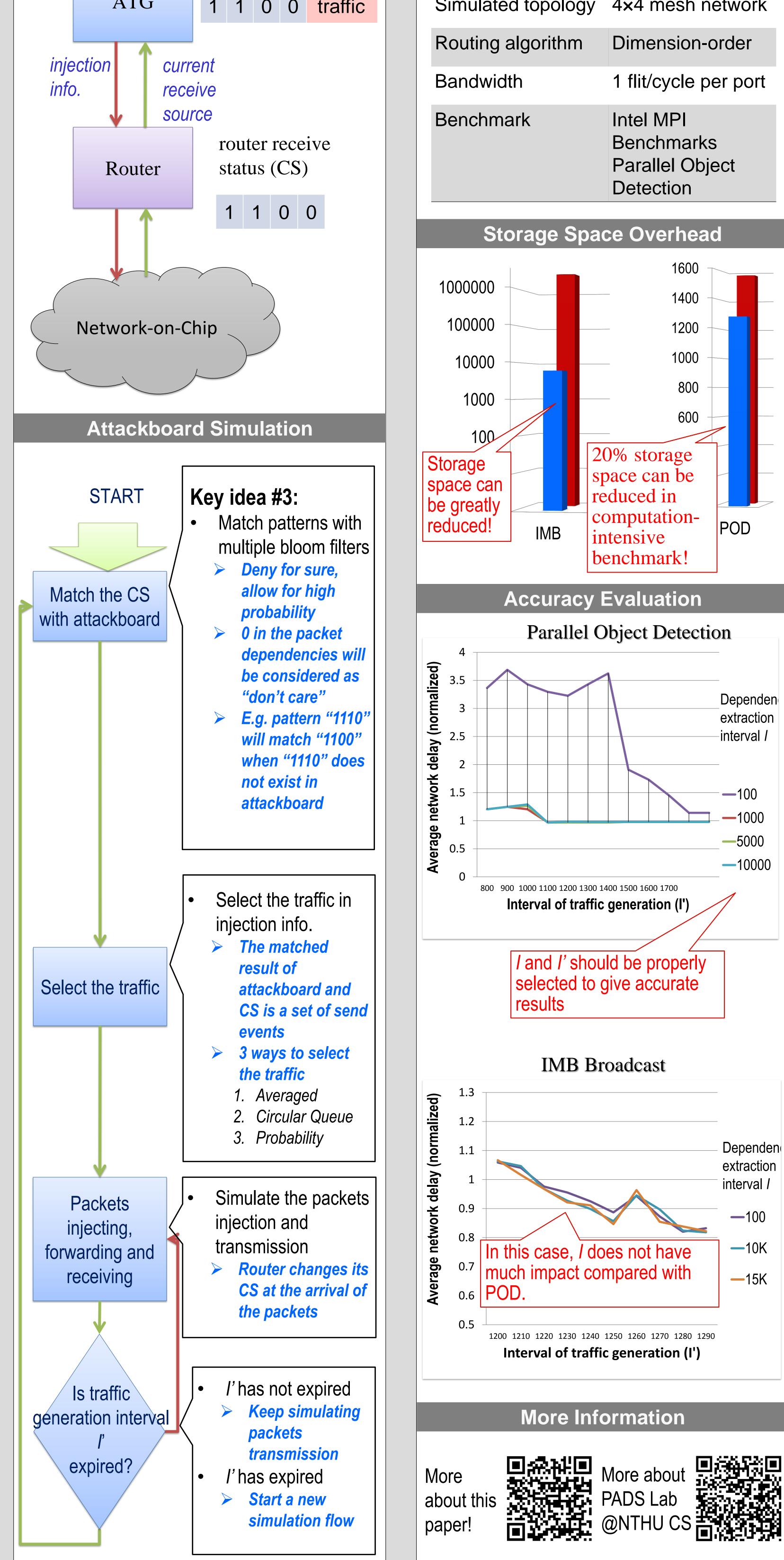
- State transitions are triggered by arrivals of packets
- > Leverage packet dependency info. in traces
- Focus on patterns of received packets

Key idea #1

- Time-driven to pattern-driven
- > Use packet arrival patterns to replace the time sequencing
- > Inject packets by the sequencing of states

PE0 PE1 PE2 PE3





	Simulated topology		4x4 mesh network		
	Routing algorithm		Dimension-order		
	Bandwidth		1 flit/cycle per port		
	Benchmark		Intel MPI Benchmarks Parallel Object Detection		
Storage Space Overhead					
	1000000 100000 10000 1000 1000 Storage space can be greatly reduced!	IMB SJ IMB	1600 1400 1200 1000 800 600 0% storage pace can be educed in omputation- itensive enchmark!	POD	

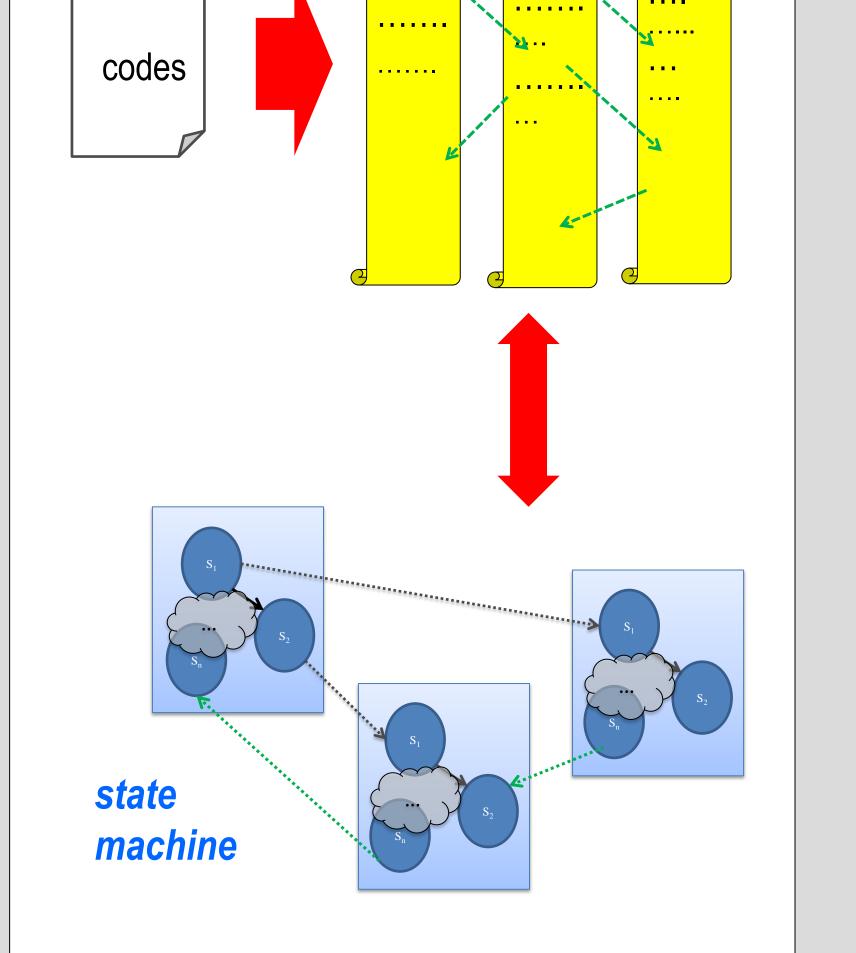
Proposal: A novel pattern-driven simulation mechanism

Key Insights

- Each PE has its own BIG trace for NoC operations
- Each BIG trace is actually a log of the execution of the corresponding *State Machine*

10KB codes may result in more than 1GB traces!

1GB trace logs



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