Computer Architecture

Fall, 2020

Week 12

2020.11.30

Group:

組員簽名：_____

[group7] (對抗賽)

1. Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-

I. Pipeline cycle time

II. Single Cycle execution time

III. Pipeline time for 1000 tasks

IV. Single cycle time for 1000 tasks

V. Speed up ratio (based on Ⅲ and Ⅳ)

VI. Throughput

Ans:

I. Pipeline Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 60, 50, 90, 80 } + 10 ns

= 90 ns + 10 ns

= 100 ns

II. Single cycle execution time for one instruction

= 60 ns + 50 ns + 90 ns + 80 ns

= 280 ns

III. Pipeline time for 1000 tasks

= Time taken for 1st task + Time taken for remaining 999 tasks

= 1 x 4 clock cycles + 999 x 1 clock cycle

= 4 x cycle time + 999 x cycle time

= 4 x 100 ns + 999 x 100 ns

= 400 ns + 99900 ns

= 100300 ns

IV. 280 ns * 1000 = 280000 ns

V. speed up ratio = 280000/100300

VI. Throughput for pipelined execution

= Number of instructions executed per unit time

= 1000 tasks / 100300 ns

[group11] (對抗賽)

2. Which of the following statements are true?

A. If two instructions try to write the register file at the same time, structural hazard occurs

B. we need to fetch the instruction from the Instruction Memory at the last stage

C. R-type instructions read the data from the Data Memory at MEM stage

D. In MIPS 5 –stage pipeline , Read registers are always done before write registers(structural hazard)

E. Pipeline rate limited by slowest stage

Ans: (a) (d) (e)

(b) first

(c) nothing is being done

[group12] (對抗賽)

3. Pipeline is a technique that can effectively (choose the correct answer(s))

(a) reduce the latency of an operation

(b) increase the throughput of instruction execution

(c) increase the clock rate

(d) reduce the CPI

Ans: (b)、(c)

[group9]

4. 為什麼 WAR 和 WAW MIPS 5-stage 的 pipeline 中不會發生?

Ans:

因為所有的 instructions 都是 5 stages，read 一定在 stage 2，write 一定在 stage 5。

[group14] (對抗賽)

5. 針對一段程式碼，沒有管線(pipeline)執行跟有管線化執行的差別，下列敘述何者錯誤？

(A) 沒有管線化執行不會發生 hazard

(B) 沒有管線化執行的效能較差 (throughput)

(C) 管線化執行能增加指令同時執行的速度(maybe throughput)

(D) 管線化執行能縮短單一指令執行的時間

Ans:

(D)單一指令的執行時間都是固定的

[group13] (對抗賽)

6. Which of the following statement is true for Pipelining?

(a) Pipeline is practical since the resources of processor can be shared by multiple instructions at the same time

(b) Pipeline is cut into five stages, which are IF, RD, EX, MEM, JUMP

(c) A structural hazard occurs when two different types of instructions trying to access the same resource of the processor

(d) By extending all types of instructions to finish after exactly five cycles, we solve the structural hazard problem

Ans:

(c), (d)

(a) since "the resources can be used by one instruction after another one used it right away"

(b) IF, ID, EX, MEM, WB

[group4] (對抗賽)

7. Consider the following MIPS assembly code and identify all pipeline hazards under the assumption that there are no pipeline optimizations implemented-including forwarding. The first column of numbers are line numbers that you can refer to in your explanation.

1. addi $3, $0, 100
2. addi $4, $0, 0
3. loop: addi $4, $4, 4
4. add $5, $4, $3
5. sw $5, 100($4)
6. addi $1, $1, -1
7. slt $2, $4, $3
8. bne $2, $0, loop
9. jr $31

Ans:

Data hazards:

(a) Line 3 needs to wait for line 2 to evaluate the value of $4 (in the first iteration)

(b) Line 4 needs to wait for line 2 to evaluate the value of $4 (every iteration)

(c) Line 5 needs to wait for line 4 to evaluate the value of $5 (every iteration)

(d) Line 8 needs to wait for line 7 to evaluate the value of $2

Control hazard:

(a) Line 8 will stall while determining if $2 is equal to $0

[group3] (對抗賽)

8. Determine whether the following statements is correct or not. If it is incorrect, correct it.

(A) Since the potential speedup equal to the stage of pipeline, more stage is better.

(B) Pipeline does improve the latency of single instruction.

(C) The latency of one stage is dominated by the most time-consuming stage.

(D) In MIPS, each instruction runs through all stages.

(E) In MIPS, the number of pipeline registers are equal

Ans:

(A): False. More stage, more hazard need to deal with. Once we counter the hazard, more stage will bring us more penalty.

(B): False. Pipeline does improve the throughput of the CPU, not the latency of single instruction.

(C): True.

(D): True.

(E): False. The number of pipeline registers are different.

[group5]

9. If a pipelined processor has 5 stage and takes 100ns to execute N instructions. How long will it take to execute 2N instructions. Assuming the clock rate is 500MHz and no pipeline stalls occur?

Ans:

cycle time = 1/(500*10^6) = *2ns*

N+4 = 100/2 => N=46

*2N time = (*246+4) * 2 = 96 * 2 = **192ns**#