CS 613200 Advanced Logic Synthesis Homework 1 (2025, Spring)

Due Date: 2025/4/9

OBJECTIVE

Based on the knowledge given in class, **evaluate** and **analyze** logic synthesis tool, SIS and ABC.

Upload the report (max 4 pages) to <u>eeclass</u> by **2025-04-9**.

INTRODUCTION

SIS (A System for Sequential Circuit Synthesis) and ABC (A System for Sequential Synthesis and Verification) are academic tools developed by UCBerkeley. They are used for synthesis and optimization of binary sequential logic circuits appearing in synchronous hardware designs.

In this project, you will use these tools to optimize circuits in logic level. Several logic optimization techniques are introduced in our class. These techniques can be applied to circuits through commands in SIS and ABC environment. To optimize a circuit with these techniques, several commands with proper parameters are executed iteratively. For different optimization objectives and for circuits with different characteristics, different scripts are used.

Reference Process:

- 1. Select a number of test benches from MCNC benchmark set (you can download it from course <u>website</u>).
- 2. Use the scripts provided in **SIS** and in **ABC** to **optimize** them (you can define new scripts by yourself).
- 3. Try to understand and explain the purpose of these scripts based on experiments.
- 4. Compare the optimization efficiency of **SIS** and **ABC** in terms of **quality** and **runtime**.

TOOL INFORMATION

- A. General Information
 You can obtain information about tools on our <u>website</u>. The
 "Description" of each tool includes a link to its explanation.
- B. NTHU CAD Severs, using host: ic51, ic55~58
- C. How to run:
 - a. Download executable file of SIS, ABC, and MCNC Benchmark from our <u>website</u>. (If you want to know more details of tool, you can download the source code)
 - b. SIS: ./sis
 - c. ABC: ./abc
 - d. MCNC Benchmark: Copy the benchmark to your working directory

About ABC9

ABC9 extends the original ABC tool with specific optimizations for XOR logic gates. It introduces a new GIA manager that natively supports XOR nodes alongside traditional AND nodes. The key innovation is the XAIG representation, which treats XOR operations as basic nodes rather than requiring multiple AND nodes. This approach improves handling of XOR-intensive circuits like encryption algorithms. Typically ABC9 commands start with "&". We encourage students to experiment with ABC9 commands and compare results with traditional approaches.

HINTS

About Tools:

- 1. <u>A Tutorial of Usage and Programming of SIS</u>
- 2. <u>A Tutorial of ABC</u>
- 3. <u>Github: ABCPaperCheck</u>

About reports:

Use any format for your assignment, here is some example about tool evaluation and analyze:

- Experimental Results of DAG-Aware AIG Rewriting
- Experimental Results of Functionally Linear Decomposition and Synthesis of Logic Circuits for FPGAs
- Are XORs in Logic Synthesis Really Necessary?

About Chatgpt:

Don't use NLP model to generate your report !!! We will use <u>AI Text Classifier</u> to check.

If you have any questions, feel free to ask TA via email~ TA: 王睿杰 | 唐梧遷 Email: <u>wrj651121@gmail.com</u> | <u>towne.cpp@gmail.com</u>